REMARKS

Claims 1-7 and 14-17 stand rejected and claim 1 stands additionally objected to. More particularly, claims 1 and 3-5 stand rejected under 35 U.S.C. 102(e) and claims 2, 6-7 and 14-17 stand rejected under 35 U.S.C. 103. Claims 8-13 and 18-21 have been allowed. Appreciation is expressed at this point for the allowance of claims 8-13 and 18-21. Applicants have amended claims 1, 16 and 17 and cancelled claims 14-15 without prejudice. Reconsideration of the application is respectfully requested. The various rejections of the claims are addressed in turn below.

Rejections Under 35 U.S.C. 102

The Examiner rejected claims 1, 3-5 under 35 U.S.C. as being anticipated by U.S. Patent No. 6,747,325 to Shih. Shih discloses forming first and second halo regions 427 and 428 using oppositely directed ion implantations.[1] However, Shih discloses the processing of a single transistor and without any masking thereof. Applicants have amended claim 1 to recite the formation of a mask on a substrate with an opening that exposes the circuit device. Applicants submit that claim 1 and claims 3-5 depending therefrom now distinguish over the teachings of Shih.

Rejections Under 35 U.S.C. 103(a)

Claim 2

Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of U.S. Patent No. 6,784,062 to Cho et al. Shih discloses a fabrication process for a thin film transistor (TFT) for controlling pixels of a TFT liquid crystal display.[2] Two embodiments are disclosed that use halo regions.[3] Interestingly, the two embodiments are described solely in the context of an N-type lightly doped drain (LDD) and a P-type halo region. There is no hint or suggestion of using anything other than an N-type LDD and a P-type halo.

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[1]Shih, col. 6, ll. 2-17.

[2]Shih, col. 1, ll. 14-18.

[3]Shih, col. 6, ll. 2-17, FIGS. 4a-4h, col. 7, ll 56-60 and FIGS. 5a-5h.

Cho et al. discloses a fabrication process to build side-by-side N-channel and P-channel transistors with halo regions using a quad implant process.[4] The stated application for the transistors in Cho et al. is random access memory.[5]

Applicants submit that there is no motivation to combine the teachings of Shih and Cho et al. as required by 35 U.S.C. 103(a). As just noted, Cho et al. discloses subject matter related to quad halo implantation in the random access memory context. Shih discloses a TFT process solely in the context of an N-type LDD and a P-type halo and for a very particularized application, namely, a pixel control for a TFT liquid crystal display. The skilled artisan would simply not be motivated to take the rather specific teachings of Shih and then turn to the otherwise disparate teachings of the Cho et al. reference and plug the same into Shih.[6]

Claims 6 and 7

The Examiner rejected claims 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Shih. For the reasons advanced above with regard to the patentability of claim 1, Applicants submit that claims 6 and 7 are similarly patentable.

Claim 14-17

The Examiner rejected claims 14-17 under 35 U.S.C. 103(a) as being unpatentable over Cho et al. in view of Shih. Applicants have cancelled claims 14-15 and amended claims 16-17 to change the dependency thereof from now-cancelled claim 14 to claim 1. Accordingly, Applicants submit that claims 16-17 are now patentable for the reasons advanced above with regard to claim 1.

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[4]Cho et al., col. 3, ll. 44-50.

[5]Cho et al., col. 2, ll. 46-59.

[6]The Examiner has asserted that Shih and Cho et al. are from the same field of endeavor. May 16, 2006 Office Action ¶7. Applicants submit that this issue is not altogether clear. As noted elsewhere herein, Shih discloses a specific transistor design for use in TFT liquid crystal displays while Cho et al. discloses transistor concepts for use in random access memory devices.

Claim Objection

The Examiner objected to claim 1 on grounds that the word "the" before the word "substrate" in the first element of claim 1 as-filed lacked antecedent basis. Applicants' amendment to claim 1 in the present paper has introduced the phrase --a substrate-- and thus eliminated the grounds for objection to claim 1.

Conclusion

For the extensive reasons advanced above, Applicants submit that claims 1-13 and 16-21 are patentable and respectfully request that a Notice of Allowability issue in due course.

Miscellaneous

The Commissioner for Patents is authorized to charge any required fees or credit any overpayment to Deposit Account No. 01-0365, Order No. AMDI:133\HON.

Respectfully submitted,

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/Timothy M. Honeycutt/

Timothy M. Honeycutt
Reg. No. 37,153
Attorney at Law
P.O. Box 1577
Cypress, Texas 77410-1577
(281) 379-7999 Voice
(281) 379-7997 Fax
timhoney@sprynet.com e-mail
Attorney for Assignee
ADVANCED MICRO DEVICES, INC.